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(54) Integrated circuit assembly having output pads with programmable characteristics and method of operation

(57) An apparatus and method of calibrating a circuit assembly (10) having an IC (14) with an output pad (20) having a number of drivers (32, 34,36,38) connected to the pad. The method includes electrically connecting the pad to an output line (132) of an external circuit, then operating the IC and measuring an electrical characteristic of the output line. Based on the electrical characteristic of the output line, an electrical component (134) is connected to the output line, and based on the electrical characteristics of the output line with the electrical component connected, the drivers are set to a selected state, which includes including enabling at least a selected one of the output pad drivers, so that the output pad is driven adequately to compensate for the electrical component on the output line.

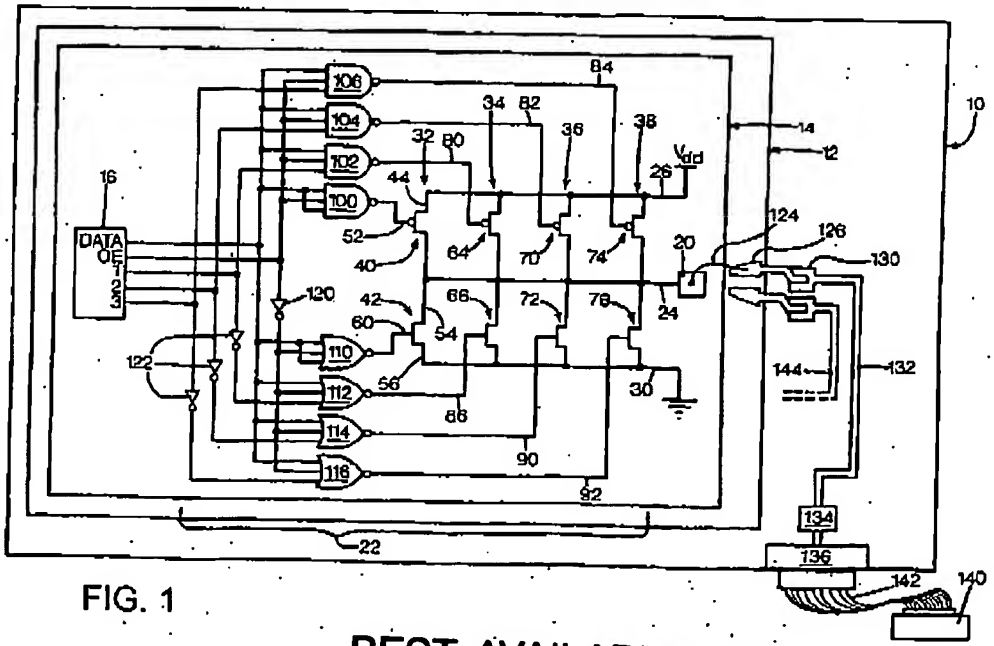

FIG. 1

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Description

Field of the Invention

[0001] This invention relates to methods and apparatus for driving an integrated circuit (IC) output pad, and more particularly to compensation for application specific electromagnetic interference (EMI) reduction circuitry.

Background and Summary of the Invention

[0002] Electronic integrated circuits are provided with output pads to which external electronic circuitry is electrically connected. Output pads may provide a logic signal of "1" or "0", or an elevated or zero voltage to indicate a logic state. To overcome the impedance of the external circuitry, each pad is provided with a driver, typically in the form of a pair of FET transistors connected in series, with the junction between the two connected to the output pad, and the remote connections of the pair connected to a power line and to ground, respectively.

[0003] ICs are typically installed on a printed circuit assembly (PCA) with other components, and other circuit assemblies or devices may be connected to the PCA. The output pad may be required to drive a load remote from the IC, after transmission via metal traces on the PCA or via other conductors. The interactions of rapidly switching signals on these traces may generate an unwanted EMI problem. While rapid switching may be desirable for high speed circuit operation, this increases EMI noise. Therefore, circuits are evaluated and provided with EMI filtration components where EMI exceeds allowable levels. However, the addition of these components on the lines driven by an output pad changes the impedance of the line, which changes the requirements on the driver on the IC. For certain applications, an IC may be custom designed to have driver capabilities at each output pad precisely matched to the intended application and PCA on which it is to be installed. This would provide driving capabilities that are adequate to overcome external impedance, yet below a level that generates excessive EMI.

[0004] However, it is impractical or cost ineffective to design an IC twice: once to prototype the system for EMI analysis, and a second time with adequate drive capabilities to accommodate EMI reduction measures. Even when computer simulations of circuit performance are adequate to predict EMI measures and design adequate drivers in a single iteration, a separate chip design is required for each product or circuit assembly on which the chip is to be used.

[0005] Existing ICs have output pads with two drivers per pad, so that a driver may be disabled during operational periods when switching noise within the IC is excessive. Such a system is disclosed in US Patent No. 5,039,878 to Anderson, the disclosure of which is incorporated herein by reference. However, such systems do not accommodate the impedance variations generated by off-chip components and simply respond to excessive noise on a ground line.

[0006] The present invention overcomes the limitations of the prior art by providing an apparatus and method of calibrating a circuit assembly having an IC with an output pad having a number of drivers connected to the pad. The method includes electrically connecting the pad to an output line of an external circuit, then operating the IC and measuring an electrical characteristic of the output line. Based on the electrical characteristic of the output line, an electrical component is connected to the output line, and based on the electrical characteristics of the output line with the electrical component connected, the drivers are set to a selected state, which includes including enabling at least a selected one of the output pad drivers, so that the output pad is driven adequately to compensate for the electrical component on the output line.

Brief Description of the Drawings

[0007] Fig. 1 is a schematic block diagram of a circuit according to a preferred embodiment of the invention.

Detailed Description of a Preferred Embodiment

[0008] Figure 1 shows a printed circuit assembly 10 on which is mounted a chip carrier 12 carrying an integrated circuit (IC) chip 14. The chip includes a microprocessor controller 16 that is interconnected to control all chip functions. An output pad 20 represents one of numerous output pads for expressing a digital signal from the chip.

[0009] A pad driver circuit 22 has an output line 24 connected to the pad, a voltage line 26 connected to a voltage source Vdd, and a ground line 30 connected to ground. The driver circuit shown has four pad driver transistor pairs 32, 34, 36, 38. Each pair includes a p-channel FET and an n-channel FET connected with the p-FET source connected to the n-FET drain, with the drain of the p-channel FET connected to Vdd line 26 and the source of the n-channel FET connected to ground 30. Pair 32 includes p-FET 40 and n-FET 42. FET 40 has a first line 44 connected to Vdd line 26, a second line 46 connected to the output line 24, and a gate 52. FET 42 has a first line 54 connected to the output line 24 and to the second line 46 of FET 40, a second line 56 connected to the ground line 30, and a gate 60.

[0010] FET pairs 34 includes a p-FET 64 and an n-FET 66, pair36 includes FETs 70 and 72, and pair 38 includes FETs 74 and 76. The p-FETs 40, 64, 70, and 74 are all connected to Vdd line 26, and n-FETs 42, 66, 72, and 76 are connected top ground line 30. The p-FETs 40, 64, 70, and 74 have respective gate lines 52, 80, 82, 84, and n-FETs 42, 66, 72, and 76 have respective gate lines 60, 86, 90, 92.

[0011] Each of the gate lines 52, 80, 82, 84 of the p-

FETs is connected respectively to the output line of a NAND gate 100, 102, 104, 106. Each of the gate lines 60, 86, 90, 92 of the n-FETs is connected respectively to the output line of a NOR gate 110, 112, 114, 116. Each of the NAND and NOR gates has three inputs: a first data input connected to a DATA line on microprocessor 16, a second enable line connected to an output enable (OE) on the microprocessor, and a control line. An inverter 120 on the OE line between the processor and the NOR gates provides an inverted OE signal, while the NAND gates directly receive the original OE signal.

[0012] A separate control line is connected to each of the NAND gates, and each line is shared with a respective NOR gate. As the enable line inverter prevents p-FETs and n-FETs from operating simultaneously, control line sharing allows simplification of the interface with the microprocessor. The processor 16 includes three control line outputs 1, 2, and 3, which is one less than the number of FET pairs. Control line 1 connects to NAND gate 102 and NOR gate 112, control line 2 connects to NAND gate 104 and NOR gate 114, control line 3 connects to NAND gate 106 and NOR gate 116. Gates 100 and 110 are wired with their control inputs directly connected to the data line so that they receive a high control bit when the data line is high. This ensures that these gates will always be on, while the others may be selectively utilized based on the processor's control bit output.

[0013] The NAND gates conventionally operate to provide a low or "0" output when all three inputs are high (causing an associated p-FET to conduct, and pulling the output line up to Vdd), and provide a high or "1" output when one or more of the inputs are low (preventing p-FET conduction). The NOR gates conventionally operate to provide a low or "0" output when one or more inputs are high (preventing an associated n-FET from conducting), and a high or "1" output when all inputs are low (pulling the output line down to ground.) Thus, when the enable line OE is high and the data line switches high (as when a "leading edge" of a digital signal occurs) any control lines at high (including the data-following control line of gate 100) will cause their associated NAND gate to send a "0", causing some p-FETs to conduct. Meanwhile, the inverter 120 on the enable line will pass a low "0" signal to the enable lines of each of the NOR gates, which are effectively enabled by a "0" and disabled by a "1". Thus, a single enable bit will affect the entire circuit simultaneously.

[0014] On the data line, a "1" effectively enables or operates the NAND gates and disables the NOR gates, while a "0" functions conversely. Consequently, the data line circuit logic prevents enablement of any p-FETs when any n-FET is enabled, and vice versa, avoiding an intolerable connection between Vdd and ground within the chip.

[0015] On each of the control lines to the NOR gates, an inverter122 takes a high control bit and inverts it to the low level needed to activate the gate, and conversely disables the selected gate when the microprocessor outputs a low control bit.

[0016] In the preferred embodiment, the FET transistors are sized in incremental multiples of two, providing a wide range of selectable aggregate effective sizes. The first p-FET 40 is the smallest size x, with p-FET 64 at 2x, p-FET 70 at 4x, p-FET 74 at 8x. Thus, with four transistors, the effective size of the transistor may range between 1x and 15x, in quantum increments of 1x, depending on which permutation of transistors is selected. In the preferred embodiment with FET 40 permanently wired to be on when enabled and data high, the possible aggregate sizes are 1x, 3x, 5x...15x. Where finer increments are desired, the first transistor may be wired with a switchable control bit. The n-FETs are similarly sized, although the number of n-FETs may differ from the number of p-FETs, as may the progression of sizes.

[0017] As long as all FET outputs connect to the output pad, the FETs need not be arranged physically or conceptually in pairs, except that at least one of each type must be provided for basic pull up and pull down functions.

[0018] The chip 12 is supported by a the chip carrier 14, and a tab or wire bond 124 connects the output pad 20 to a land 126 on the carrier. A multitude of other wire bonds connect other pads to other lands. The lands of the chip carrier are electrically connected to conductive terminals 130 on the printed circuit assembly 10 by conventional soldered connections. A conductive trace 132 extends to a filter component 134 near the PCA periphery, where a connector module 136 is connected to the trace, and to an external component or instrument 140 via a cable 142. The filter is typically a resistor, a resistor/capacitor, or a ferrite bead.

[0019] The selectable controls on the effective size of the pad drivers is used to optimize the driver strength for a specific application of the chip. In each application, the driver controls are adjusted to compensate for impedances that occur outside the chip, primarily on the PCA. On the PCA, an adjacent trace 144 near trace 132 may exhibit capacitive and inductive coupling with trace 132, generating unwanted EMI noise on either line in response to switching on the other. Either trace may also be subject to stray capacitances. Accordingly, after a prototype system is assembled, these EMI problems may be detected and identified. To cure the EMI problems, an appropriate filter 134 is connected to the trace 132 near the connector, to reduce EMI on the signal expressed at the connector to the external device 140. Typically, such filters slow the switching speed of the pad drivers, and additional transistor size is required to compensate. However, a large transistor size adequate for a heavily filtered trace will generate excessive noise on lines or in other applications of the same chip where filtering was not required. Therefore, the combination of transistors may be selected to provide adequate switching speed. In the design process, filtering and driver control codes may be iterated to optimize the settings.

[0020] Normally, after the driver control settings are established for each pad, they remain constant throughout use, avoiding the need for sensors, and reducing the demand on the microprocessor during operation. However, where these are not a concern, the system may include noise sensors on the chip or on the PCA circuitry to provide feedback to the microprocessor to enable it to adjust drive levels during normal operation.

[0021] To further reduce noise concerns, the microprocessor may trigger the control gates with pulses that are not simultaneous, but which may provide a stair step turn on of the FETs, or which may be slightly randomized. The control bits may be manipulated by an algorithm of the user's choice.

[0022] While the above is discussed in terms of preferred and alternative embodiments, the invention is not intended to be so limited.

Claims

1. A method of operating a circuit comprising the steps:

   providing output pad (20) with at least a first driver and a second driver connected to the pad;
   determining the output requirements of the pad;
   based on the determined output requirements, enabling a selected set of the drivers (32, 34,36,38) to drive the pad; and
   operating the circuit while maintaining the drivers in the selected state of enablement, such that the operating characteristics remain unchanged during operation.

2. A method according to claim 1 wherein determining the output requirements includes measuring EMI on a circuit portion (132) connected to the pad, and connecting an EMI control component (134) to the circuit portion.

3. A method according to claim 1 or claim 2 wherein connecting an EMI control component includes changing the impedance of the circuit portion.

4. A method according to any one of claims 1 to 3 wherein the output pad has at least three drivers, such that multiple permutations of the drivers may be selected.

5. A method according to any one of claims 1 to 4 wherein setting the drivers includes setting at least one of the drivers in a disabled state, and at least one of the drivers in an enabled state.

6. A method according to any one of claims 1 to 5 wherein the IC includes a plurality of output pads (20), and including setting the drivers of at least some of the pads to a different state than the drivers of others of the pads, such that different pads are driven differently.

7. An electronic circuit comprising:

   an IC (14) having an output pad (20);
   a plurality of drivers (32, 34,36,38) on the IC connected to the output pad;
   a controller (16) on the IC connected to each of the drivers and operable to switch each of the drivers independently between an enabled state and a disabled state;
   an external circuit having an output line (132) electrically connected to the pad;
   an EMI control component (134) connected to the output line;
   the controller including selection means for setting the drivers in a selected state, based on the impedance of the output line with the EMI control component connected.

8. A circuit according to claim 7 wherein the controller (16) is a microprocessor.

9. A circuit according to claim 7 or claim 8 wherein the controller includes means for maintaining the drivers in the selected state during operation of the circuit, such that the drivers may be calibrated and set to a permanent setting.

10. A circuit according to any one of claims 7 to 9 wherein the EMI control component (134) is a filter.

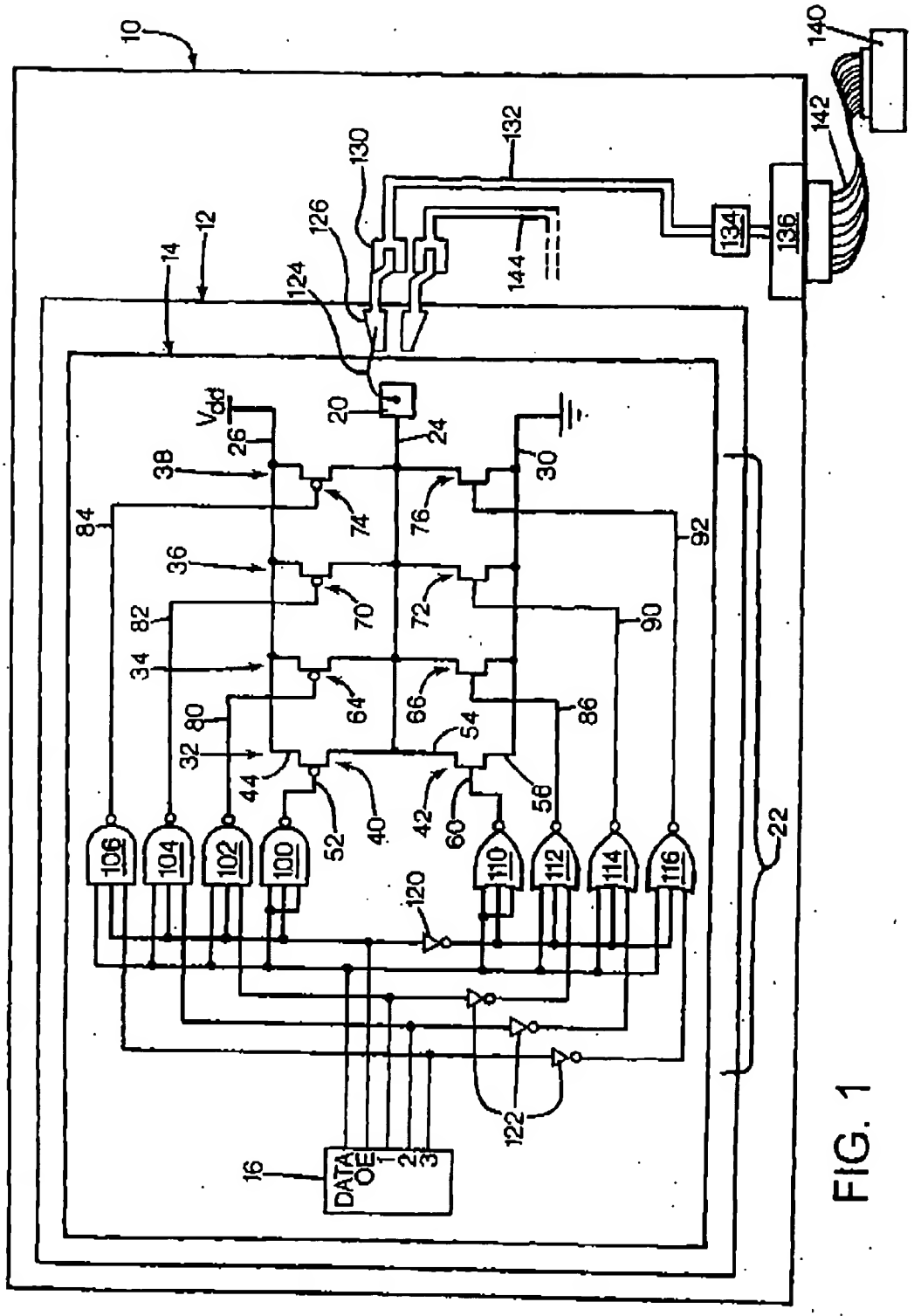
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FIG. 1

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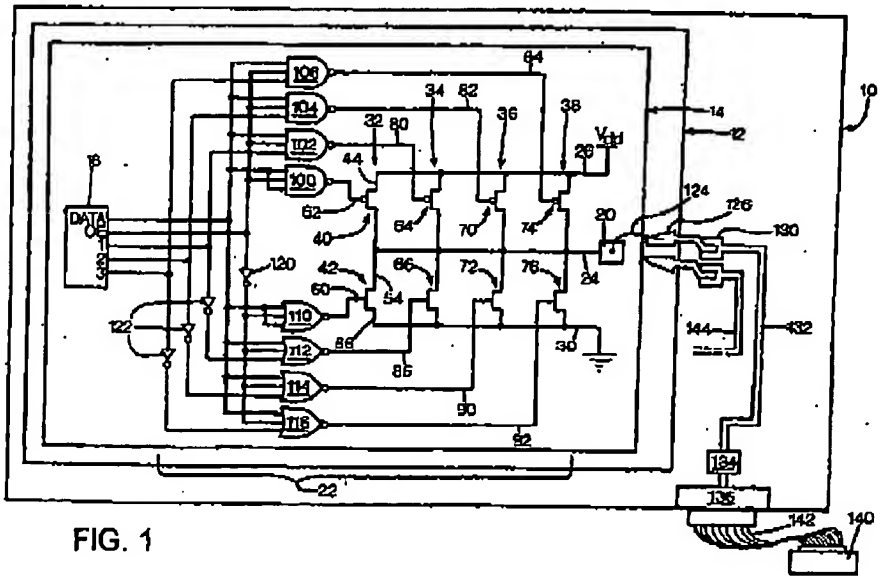

FIG. 1

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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 8438

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 677 639 A (MASIEWICZ JOHN CHESTER) 14 October 1997 (1997-10-14) * column 1, line 20 - column 3, line 33; figures 1A,1B,2A,2B * * column 3, line 64 - column 4, line 47 * * column 3, line 50 - column 7, line 35; figures 3A,3B,4A,4B *	1,4,5,7, 9	H03K19/0185 H03K19/00 H03K19/003 H03K17/16
X A	EP 0 463 316 A (IBM) 2 January 1992 (1992-01-02) * column 8, line 41 - line 54 *	1,5,7,9, 10 2-4	
X	US 5 153 450 A (RUETZ J ERIC) 6 October 1992 (1992-10-06) * figure 2 *	1,4,5	
X	EP 0 778 673 A (SIEMENS AG) 11 June 1997 (1997-06-11) * column 1, line 1 - line 22 * * figures 3-6 *	1,4-6	
A	EP 0 490 654 A (TEXAS INSTRUMENTS INC) 17 June 1992 (1992-06-17) * the whole document *	2,3,7	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 December 1999	Feuer, F

CATEGORY OF CITED DOCUMENTS

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08-12-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5677639 A	14-10-1997	NONE	
EP 0463316 A	02-01-1992	US 5134311 A	28-07-1992
		DE 69120606 D	08-08-1996
		DE 69120606 T	23-01-1997
		JP 2700042 B	19-01-1998
		JP 6260922 A	16-09-1994
US 5153450 A	06-10-1992	EP 0523833 A	20-01-1993
		JP 6196981 A	15-07-1994
		KR 9505019 B	17-05-1995
		US 5319258 A	07-06-1994
EP 0778673 A	11-06-1997	DE 19545904 A	12-06-1997
		US 5834955 A	10-11-1998
EP 0490654 A	17-06-1992	US 5153457 A	06-10-1992
		JP 4302526 A	26-10-1992

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